

Overview

The X2VDDR module is a volatile credit card sized VIRTEX-II™ FPGA building block. Its in-system programmable configuration flash memory enables stand-alone applications as well as host-controlled systems. 32 Mbytes of DDR SDRAM are connected to the FPGA and can easily be used by including a SDRAM controller netlist into the design (sold separately).

Summary of XV2DDR Features

XILINX VIRTEX-II FPGA

XC2V1000-5FG456C

- 1 Million System Gates
- CLB array 40 x 32
- Slices 5,120
- Maximum Distributed RAM 160 kBits
- Multiplier Blocks 40
- SelectRam Blocks (18-kBit each) 40
- DCMs 8
- IP-Immersion Architecture

Double Data Rate (DDR) SDRAM

Micron MT46V16M16-75

- Capacity 256Mb (32 Mbyte)
- Organization 16M x 16
- Quad bank, 2.5V, SSTL_2
- Cycle time 7.5 ns (133MHz)

ISP Configuration PROM

XC18V04

- stand-alone configuration of the FPGA
- Endurance of 20,000 program/erase cycles
- IEEE Std 1149.1 boundary-scan (JTAG)

Two independent Oscillators

- 100 MHz and 40 MHz

Battery backup of DES encryption keys

- Protect your designs from getting cloned

Peripheral devices

- user switches 4
- user Leds 2
- Configuration-Done Led
- Reconfigure Pushbutton

Jumper selectable bank I/O voltages

- 2,5 Volt / 3,3 Volt

Single power supply

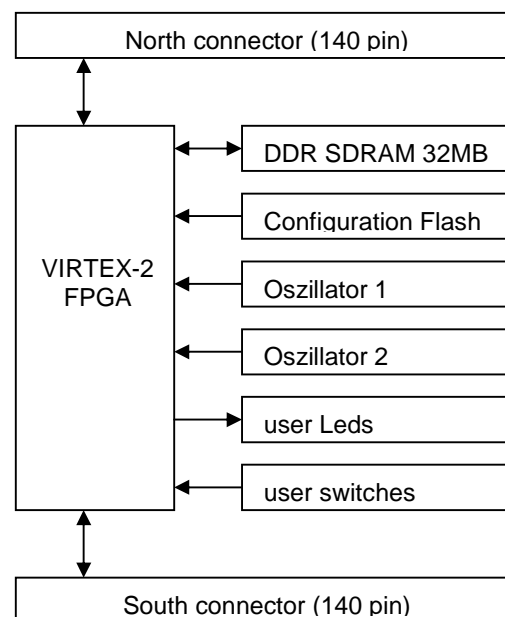
- 3,3 Volt

General Description

The XV2DDR Plug-in module is a complete solution for products that require rapid time-to-market. It provides a cost-effective, quick and easy way to integrate a 1 Million gate Virtex-II™ FPGA together with 32 MBytes of fast DDR SDRAM into the user's system. With its dimensions of only 64,13 x 55,25 mm, it fits even small size demands.

Two main connectors with 140 pins each, make integration into larger systems easy. FPGA configuration can take place self-triggered after powering the module. A Flash memory is integrated to store the configuration data permanently. Other configuration options include JTAG and fast SelectMap mode.

Block Diagram



Virtex-II™ device

Virtex-II FPGAs are loaded with the features that advanced designs require such as XCITE technology (Digitally Controlled Impedance), advanced Digital Clock Managers (DCMs), embedded hardware multipliers, and System I/O capable of supporting 19 single-ended or 5 differential standards and 840 Mb/s LVDS on any I/O pair.

Virtex-II FPGAs provide a solution that combines all of the features necessary for sophisticated System on a Chip (SoC) design in a single programmable device.

For detailed information look at the Virtex-II datasheet or visit the Xilinx webpage at www.xilinx.com.

DDR SDRAM MT46V16M16 – 4 Meg x 16 x 4 banks

- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two – one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto Refresh and Self Refresh Modes
- 2.5V I/O (SSTL_2 compatible)
- Concurrent auto precharge option is supported

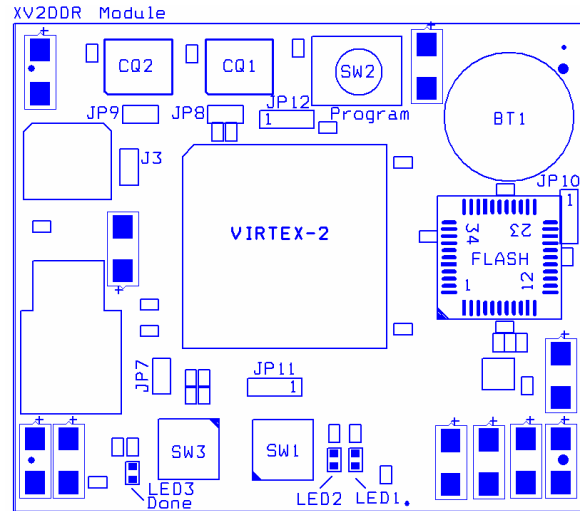
Configuration Flash memory

XC18V04: In-system programmable 3.3V PROM for configuration of Xilinx FPGAs

In-System Programmable PROMs can be programmed in-system via the standard 4-pin JTAG protocol. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The Xilinx development system provides the programming data sequence using either Xilinx JTAG Programmer software and a download cable, a third-party

JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence.

Board Layout



The XV2DDR Module is equipped with two 140-pin Tyco/AMP SMD-receptacles with 0.8mm pitch and 5mm height (AMD part number: 177983-6).

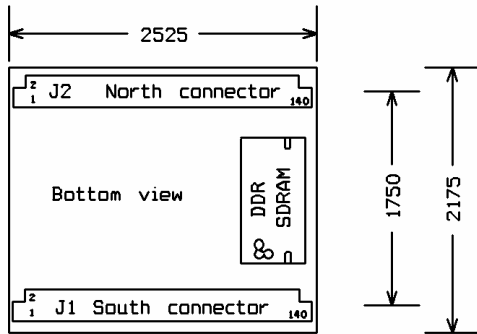
Matching connector part number:

AMD 177984-6	5 mm height
AMD 179029-6	6 mm height
AMD 179030-6	7 mm height
AMD 179031-6	8 mm height

The horizontal distance between connectors J1 and J2 is 1750 mil (44,45 mm).

Important: Please note, that the pin numbering of the XV2DDR module differs from the pin numbering conventions of the AMD/Tyco datasheet ! XV2DDR Pin 140 is marked as pin 1 on the connectors.

J1 (South) and J2 (North) connectors



View to the bottom of the module to clarify the connectors orientation and pin numbering scheme.

User Leds

The XV2DDR module provides 2 user Leds. An active high signal is required to drive the Leds. The Leds can be driven by either I/O voltage (2.5V / 3.3V).

User Led	Virtex-2 Pin	Signal name	Bank number
Led 1	AB13	ULED1	4
Led 2	V12	ULED2	4

User Switches

The XV2DDR module provides 4 user DIP-switches. The associated Virtex Pin is pulled low when a switch is ON. When the switch is OFF, the pin is open. Therefore IOB pull-ups are required to use the switch signals.

User switch	Virtex-2 Pin	Signal name	Bank number
Switch 1	V13	USW1	4
Switch 2	W13	USW2	4
Switch 3	Y13	USW3	4
Switch 4	AA13	USW4	4

I/O Voltages and Bank Layout

The bank I/O voltage of the North and South connector signals can be selected independently.

North connector I/O voltage select

JP 11 Position	North connector I/O voltage
1 – 2	2,5 Volt
2 – 3	3,3 Volt

1 – 2	2,5 Volt
2 – 3	3,3 Volt

South connector I/O voltage select

JP 12 Position	South connector I/O voltage
1 – 2	2,5 Volt
2 – 3	3,3 Volt

Virtex-2 Bank layout

Bank No.	Connection	I/O voltage
0	South connector	Selectable (2,5 / 3,3 V)
1	DDR SDRAM	2,5 Volt
2	South connector	Selectable (2,5 / 3,3 V)
3	DDR SDRAM	2,5 Volt
4	North connector	Selectable (2,5 / 3,3 V)
5	North connector	Selectable (2,5 / 3,3 V)
6	North connector	Selectable (2,5 / 3,3 V)
7	South connector	Selectable (2,5 / 3,3 V)

DCI Resistors

Virtex-II DCI provides controlled impedance drivers and on-chip termination for single-ended I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards. When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

Please refer to the Virtex-II datasheet for details. The XV2DDR module uses 50 Ohm resistors on the appropriate FPGA pins to make the DCI feature available. On request the board is available with other resistor values.

50 Ohm Resistors are connected to pins:

A5 / B5	Bank 0
E18 / F18	Bank 2
W17 / Y17	Bank 4
V7 / V6	Bank 5
Y1 / Y2	Bank 6
C2 / C1	Bank 7

DES Bitstream protection

Backup Battery for DES keys

Battery BT1 provides the power needed to backup the Virtex-2 DES keys. The expected lifetime of the battery is minimum 10 years. The DES keys are used to protect bitstreams from being cloned and reused without authorization. Please check the appropriate Appnotes on the Xilinx website (www.xilinx.com) before generating DES protected bitstreams. The battery is connected to Pin A21 of the Virtex-2 device.

FPGA Configuration

Configuration options

The XV2DDR configuration options are selected by DIP-switch SW3 and JP 10

SW3 Position			Configuration mode
1 (M0)	2 (M1)	3 (M2)	
OFF	OFF	OFF	Slave Serial
OFF	OFF	ON	Slave SelectMap
OFF	ON	OFF	JTAG
ON	OFF	OFF	Master SelectMap
ON	ON	ON	Master Serial

Pre-Configuration Pull up

Switch number 4 on SW3 defines the I/O Pin behavior prior to configuration:

SW3 switch 4 Position	Pre-configuration Pull-up
OFF	Pull-up disabled
ON	Pull-up activated

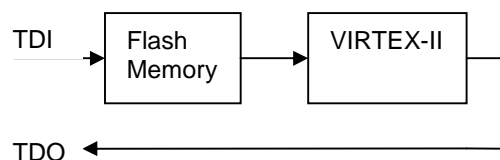
SelectMap ChipSelect

JP 7 Position	Signal SM_CS _n
Open	Sourced by North Con. Pin 54
Closed	Tied to GND

Flash memory Reset source

JP 10 Position	Flash OE/Reset
1 -2	SelectMap and Serial Slave
2 -3	All other modes

JTAG Configuration



A XILINX download cable can be used to program the flash memory and/or to configure the FPGA. The cable must be connected to the appropriate pins on the North Connector. The GND and VCC pins of the download cable must be connected to the V3 and GND voltage levels of the XV2DDR module.

North Connector Pin	Signal
104	TDI
106	TDO
108	TMS
110	TCK

Sample JTAG configuration flow

Even if you only want to program the flash memory or to download a bitstream to the FPGA you will need both, a PROM file *.mcs (with startup clock set to CCLK) and a FPGA bitstream file *.bit (with startup clock set to JTAG).

The following explanations are based on Xilinx ISE software with all options set to default. Other environments may require different steps.

1. Generate Flash memory programming file

Set the properties of the "Generate programming file" process by right-clicking on it. Set the startup clock on property page startup options to CCLK. Now run the process. Then click on "Generate Prom File".

Set the Prom properties (File->Prom Properties) to Single Prom, Serial, XC18V04, MCS-86,

checksum FF and save those as default. Click OK.
 Then click on File->Create Prom. Save it as mydesign.pdr. This will generate several files including the mydesign.mcf file we need. Close the window.

2. Generate FPGA Bit file

Right-click on “Generate Programming File” again. and change the startup clock to JTAG clock. Click OK. Run the “Generate Programming File” process again.
 The newly created mydesign.bit file has an JTAG startup clock and is for downloading in the FPGA. DONT click on “generate Prom file now !

3. Configure device

Connect the download cable and set the XV2DDR jumpers to:
 JP10: 2-3, JP7: Close, SW3: OFF-ON-OFF-XXX. (The XXX position defines whether to use pre-configuration pull-up resistors on the IOBs or not).
 Click on “Configure device” and then on “File->Initialize chain”. You should find the XC18V04 and the FPGA. You will be prompted to assign a file to each. Assign mydesign.mcs to the XC18V04 and mydesign.bit to the FPGA.
 Then right-click on whichever chip you wish to program and program it.

FPGA configuration by Flash Memory.

If you checked “parallel mode” when programming the XC18V04, SW3 must be set to Slave Select Map mode (OFF-OFF-ON-DONTCARE) otherwise to Master Serial mode (ON-ON-ON-DONTCARE). Press SW2 or recycle power to initiate the configuration of the FPGA based on the contents of the Flash.

Done Led

Led3 is connected to the DONE signal of the FPGA. It will light up when the FPGA was configured successfully. If the Done Led lights up, but the design doesn't start to work, one of the first things to check is the proper Startup-Clock option.

FPGA Clock sources

Two oscillators (CQ1 and CQ2) can be used as internal clock sources in addition to external supplied clock signals.

XV2 Pin	Clock source
B11	CQ1 80 MHz (default)
A11	CQ2 40 MHz (default)

Please check the actual frequency printed on top of the oscillators. The module can be equipped with alternate frequencies on request.

To disable unused clock oscillators Jumper 8 and 9 can be used.

Jumper	Description
JP-8	Set jumper to disable CQ1
JP-9	Set jumper to disable CQ2

DDR SDRAM

The XV2DDR module is equipped with an Micron Double Data Rate (DDR) SDRAM. part number: MT46V16M16-75
 – Capacity 256Mb (32 Mbyte)
 – Organization 16M x 16
 – Quad bank, 2.5V, SSTL_2
 – Cycle time 7.5 ns (133MHz)

Memory bandwidth

The peak bandwidth of the device is 532 MByte/s. (133 MHz * 2 (DDR) * 16 Bits).

Memory controller

To make use of the DDR SDRAM, a memory controller is needed. The Xilinx website provides application notes and sample code for DDR memory controllers. Many IP vendors offer ready-to-use solutions. In addition, Cesium provides a netlist that implements an extremely easy-to-use controller (sold separately). The user interface behaves like an SRAM interface (Address, Data, Read, Write) with an additional “busy” signal. Any complexity (Precharge, open and close banks, refresh, ...) is hidden from the user. The drawback of this solution is the suboptimal usage of memory bandwidth. With the current version (as of June 2002), a bandwidth of 70 Mbytes/s @ 80 MHz system-clock frequency has been reached. 116 Mbytes @ 133 MHz should be possible. Please contact CESYS (support@cesys.com) to obtain the latest information and pricing.

Pinout and connections

J1 South Connector

J1 Pin	XV2 Pin	Signal name	Bank
1	-	V3	-
2	-	V3	-
3	-	GND	-
4	E6	IO_L01N_7	7
5	E5	IO_L01P_7	7
6	D2	IO_L03N_7	7
7	D1	IO_L03P_7/VREF_7	7
8	E4	IO_L04N_7	7
9	E3	IO_L04P_7	7
10	E2	IO_L06N_7	7
11	E1	IO_L06P_7	7
12	F5	IO_L19N_7_NC	7
13	G5	IO_L19P_7_NC	7
14	F4	IO_L21N_7_NC	7
15	F3	IO_L21P_7/VREF_7_NC	7
16	-	GND	
17	F2	IO_L22N_7_NC	7
18	F1	IO_L22P_7_NC	7
19	G4	IO_L24N_7_NC	7
20	G3	IO_L24P_7_NC	7
21	G2	IO_L43N_7	7
22	G1	IO_L43P_7	7
23	H5	IO_L45N_7	7
24	J6	IO_L45P_7/VREF_7	7
25	-	GND	
26	H4	IO_L46N_7	7
27	H3	IO_L46P_7	7
28	H2	IO_L48N_7	7
29	H1	IO_L48P_7	7
30	J4	IO_L49N_7_NC	7
31	J3	IO_L49P_7_NC	7
32	J2	IO_L51N_7_NC	7
33	J1	IO_L51P_7/VREF_7_NC	7
34	J5	IO_L52N_7_NC	7
35	K5	IO_L52P_7_NC	7
36	K6	IO_L54N_7_NC	7
37	L6	IO_L54P_7_NC	7
38	-	GND	
39	K4	IO_L91N_7	7
40	K3	IO_L91P_7	7
41	K2	IO_L93N_7	7
42	K1	IO_L93P_7/VREF7	7
43	L5	IO_L94N_7	7
44	L4	IO_L94P_7	7
45	L3	IO_L96N_7	7

J1 Pin	XV2 Pin	Signal name	Bank
46	L2	IO_L96P_7	7
47	B4	IO_L01N_0	0
48	A4	IO_L01P_0	0
49	C4	IO_L02N_0	0
50	C5	IO_L02P_0	0
51	-	GND	-
52	D6	IO_L04N_0/VREF_0	0
53	C6	IO_L04P_0	0
54	B6	IO_L05N_0	0
55	A6	IO_L05P_0	0
56	E7	IO_L06N_0	0
57	E8	IO_L06P_0	0
58	D7	IO_L21N_0_NC	0
59	C7	IO_L21P_0/VREF_0_NC	0
60	B7	IO_L22N_0	0
61	A7	IO_L22P_0	0
62	-	GND	-
63	D8	IO_L24N_0_NC	0
64	C8	IO_L24P_0_NC	0
65	B8	IO_L49N_0_NC	0
66	A8	IO_L49P_0_NC	0
67	E9	IO_L51N_0_NC	0
68	F9	IO_L51P_0/VREF_0_NC	0
69	D9	IO_L52N_0_NC	0
70	C9	IO_L52P_0_NC	0
71	-	GND	-
72	B9	IO_L54N_0_NC	0
73	A9	IO_L54P_0_NC	0
74	E10	IO_L91N_0/Vref_0	0
75	F10	IO_L91P_0	0
76	D10	IO_L92N_0	0
77	C10	IO_L92P_0	0
78	B10	IO_L93N_0	0
79	A10	IO_L93P_0	0
80	E11	IO_L94N_0/VREF_0	0
81	F11	IO_L94P_0	0
82	-	GND	-
83	D11	IO_L95N_0/GCLK7P	0
84	C11	IO_L95P_0/GCLK6S	0
85	C21	IO_L01N_2	2
86	C22	IO_L01P_2	2
87	D21	IO_L03N_2	2
88	D22	IO_L03P_2/VREF_2	2
89	E19	IO_L04N_2	2
90	E20	IO_L04P_2	2
91	-	GND	-
92	E21	IO-L06N_2	2
93	E22	IO_L06P_2	2
94	F19	IO_L19N_2_NC	2
95	F20	IO_L19P_2_NC	2
96	F21	IO_L21N_2-NC	2
97	F22	IO_L21P_2/VREF_2NC	2
98	G18	IO_L22N_2_NC	2
99	H18	IO_L22P_2_NC	2

J1 Pin	XV2 Pin	Signal name	Bank
100	G19	IO_L24N_2_NC	2
101	G20	IO_L24P_2_NC	2
102	-	GND	-
103	G21	IO_L43N_2	2
104	G22	IO_L43P_2	2
105	H19	IO_L45N_2	2
106	H20	IO_L45P_2/VREF_2	2
107	H21	IO_L46N_2	2
108	H22	IO_L46P_2	2
109	J17	IO_L48N_2	2
110	J18	IO_L48P_2	2
111	-	GND	-
112	J19	IO_L49N_2_NC	2
113	J20	IO_L49P_2_NC	2
114	J21	IO_L51N_2_NC	2
115	J22	IO_L51P_2/VREF_2_NC	2
116	K17	IO_L52N_2_NC	2
117	K18	IO_L52P_2_NC	2
118	K19	IO_L54N_2_NC	2
119	K20	IO_L54P_2_NC	2
120	K21	IO_L91N_2	2
121	K22	IO_L91P_2	2
122	-	GND	-
123	L17	IO_L93N_2	2
124	L18	IO_L93P_2/VREF_2	2
125	L19	IO_L94N_2	2
126	L20	IO_L94P_2	2
127	L21	IO_L96N_2	2
128	L22	IO_L96P_2	2
129			
130			
131			
132			
133		Reserved pins	
134		Reserved pins	
135			
136			
137	-	GND	
138	-	GND	
139	-	V3	
140	-	V3	

Table 1

J2 North Connector

J2 Pin	XV2 Pin	Signal name	Bank
1	-	V3	
2	-	V3	
3	-	GND	
4	-	GND	
5	-	GND	
6	-	GND	
7	-	GND	
8	-	DONE	
9	U5	IO_L01N_6	6
10	V5	IO_L01P_6	6
11	V3	IO_L03N_6/VREF_6	6
12	V4	IO_L03P_6	6
13	W1	IO_L04N_6	6
14	W2	IO_L04P_6	6
15	U3	IO_L06N_6	6
16	-	GND	6
17	U4	IO_L06P_6	6
18	V1	IO_L19N_6_NC	6
19	V2	IO_L19P_6_NC	6
20	U1	IO_L21N_6/VREF_6_NC	6
21	U2	IO_L21P_6_NC	6
22	R5	IO_L22N_6_NC	6
23	T5	IO_L22P_6_NC	6
24	T3	IO_L24N_6_NC	6
25	-	GND	
26	T4	IO_L24P_6_NC	6
27	T1	IO_L43N_6	6
28	T2	IO_L43P_6	6
29	R3	IO_L45N_6/VREF_6	6
30	R4	IO_L45P_6	6
31	R1	IO_L46N_6	6
32	R2	IO_L46P_6	6
33	P5	IO_L48N_6	6
34	P6	IO_L48P_6	6
35	P3	IO_L49N_6_NC	6
36	P4	IO_L49P_6_NC	6
37	P1	IO_L51N_6/VREF_6_N C	6
38	-	GND	
39	P2	IO_L51P_6_NC	6
40	N5	IO_L52N_6_NC	6
41	N6	IO_L52P_6_NC	6
42	N3	IO_L54N_6_NC	6
43	N4	IO_L54P_6_NC	6
44	N1	IO_L91N_6	6
45	N2	IO_L91P_6	6
46	M5	IO_L93N_6/VREF_6	6
47	M6	IO_L93P_6	6
48	M3	IO_L94N_6	6
49	M4	IO_L94P_6	6
50	M1	IO_L96N_6	6
51	-	GND	
52	M2	IO_L96P_6	6

J2 Pin	XV2 Pin	Signal name	Bank
53	-	SM_RDWRn	
54	-	SM_CSn	
55	-	SM_D6	
56	-	SM_D7	
57	-	SM_D4	
58	-	SM_D5	
59	AB5	IO_L04N_5	5
60	AA3	IO_L04P_5/VREF_5	5
61	Y6	IO_L06N_5	5
62	-	GND	
63	W6	IO_L06P_5	5
64	AB6	IO_L19N_5_NC	5
65	AA6	IO_L19P_5_NC	5
66	Y7	IO_L21N_5/VREF_5_N C	5
67	W7	IO_L21P_5_NC	5
68	AB7	IO_L22N_5_NC	5
69	AA7	IO_L22P_5_NC	5
70	U9	IO_L24N_5_NC	5
71	-	GND	
72	V8	IO_L24P_5_NC	5
73	Y8	IO_L49N_5_NC	5
74	W8	IO_L49P_5_NC	5
75	AB8	IO_L51N_5_VREF_5_N C	5
76	AA8	IO_L51P_5_NC	5
77	Y9	IO_L52N_5_NC	5
78	W9	IO_L52P_5_NC	5
79	AB9	IO_L54N_5_NC	5
80	AA9	IO_L54P_5_NC	5
81	V10	IO_L91N_5	5
82	-	GND	
83	V9	IO_L91P_5/VREF_5	5
84	Y10	IO_L92N_5	5
85	W10	IO_L92P_5	5
86	AB10	IO_L93N_5	5
87	AA10	IO_L93P_5	5
88	U11	IO_L94N_5	5
89	U10	IO_L94P_5/VREF_5	5
90	W11	IO_L95N_5/GCLK5S	5
91	-	GND	
92	V11	IO_L95P_5/GCLK4P	5
93	AA11	IO_L96N_5/GCLK7S	5
94	Y11	IO_L96P_5/GCLK6P	5
95	AB19	SM_DOUT_BUSY	
96	AA19	INITn	
97	V18	FPGA_BITSTREAM	
98	-	SM_D1	
99	-	SM_D2	
100	-	SM_D3	
101	-	DONE	
102	-	GND	
103	-	PROGRAMn	
104	-	TDI	
105	-	FPGA_CCLK	
106	-	TDO	

J2 Pin	XV2 Pin	Signal name	Bank
107	AA18	IO_L04N_4/VREF_4	4
108	-	TMS	
109	AB18	IO_L04P_4	4
110	-	TCK	
111	-	GND	
112	AA17	IO_L06N_4	4
113	AB17	IO_L06P_4	4
114	V16	IO_L19N_4-NC	4
115	V15	IO_L19P_4_NC	4
116	W16	IO_L21N_4_NC	4
117	Y16	IO_L21P_4/VREF_4_NC	4
118	AA16	IO_L22N_4_NC	4
119	AB16	IO_L22P_4_NC	4
120	W15	IO_L24N_4_NC	4
121	Y15	IO_L24P_4_NC	4
122	-	GND	
123	AA15	IO_L49N_4_NC	4
124	AB15	IO_L49P_4_NC	4
125	U14	IO_L51N_4_NC	4
126	V14	IO_L51P_4/VREF_4_NC	4
127	W14	IO_L52N_4_NC	4
128	Y14	IO_L52P_4_NC	4
129	AA14	IO_L54N_4_NC	4
130	AB14	IO_L54P_4_NC	4
131	U13	IO_L91N_4/VREF_4	4
132	U12	IO_L94N_4/VREF_4	4
133	W12	IO_L95N_4/GCLK3S	4
134	Y12	IO_L95P_4/GCLK2P	4
135	AA12	IO_L96N_4/GCLK1S	4
136	AB12	IO_L96P_4/GCLK0P	4
137	-	GND	
138	-	GND	
139	-	V3	
140	-	V3	

Table 2

DDR SDRAM Connections

DDR SDRAM Pin	Virtex-2 Pin	Signal	Bank
29	B18	MEMA0	1
30	A18	MEMA1	1
31	B17	MEMA2	1
32	A17	MEMA3	1
35	N17	MEMA4	3
36	P18	MEMA5	3
37	P17	MEMA6	3
38	M18	MEMA7	3
39	M19	MEMA8	3
40	M20	MEMA9	3
28	A19	MEMA10_AP	1
41	N18	MEMA11	3
42	N20	MEMA12	3
2	Y21	MEMD0	3
4	Y22	MEMD1	3
5	W21	MEMD2	3
7	V21	MEMD3	3
8	V22	MEMD4	3
10	U21	MEMD5	3
11	U22	MEMD6	3
13	T21	MEMD7	3
54	R20	MEMD8	3
56	R19	MEMD9	3
57	T20	MEMD10	3
59	T19	MEMD11	3
60	U19	MEMD12	3
62	V20	MEMD13	3
63	V19	MEMD14	3
65	W20	MEMD15	3
26	M21	MEMBA0	3
27	B19	MEMBA1	1
23	N21	MEMRASn	3
22	P21	MEMCASn	3
21	R22	MEMWEn	3
20	R21	MEMLDM	3
47	T22	MEMUDM	3
24	N22	MEMCSn	3
44	N19	MEMCKE	3
16	P20	MEMLDQS	3
51	P19	MEMUDQS	3
45	D12	MEMCK	1
46	E12	MEMCKn	1
49	F13	Feedback of MEMCK	1

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